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6. AUTHOR(S)

D.S. Whitefield, C.J. Wei, J.C.M. Hwang

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Lehigh University  
Packard Laboratory #19  
Bethlehem, PA 18015

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13. ABSTRACT (Maximum 200 words)

Heterojunction bipolar transistors have been characterized up to 40GHz. In addition to direct current-voltage and high frequency small signal measurements, power and harmonic characterization has been performed. The measurement results were fitted to a ten-element equivalent circuit model in which only three elements were allowed to vary with bias. This bias dependant model is accurate to within 2% over the entire bias range and is the first step toward a true large-signal model. The power and harmonic characteristics of the heterojunction bipolar transistor can also be accurately modeled with increasing number of both bias-dependent and fixed elements. Pulsed DC and thermal measurements have also been accomplished to determine the junction temperature and understand its effects on device characteristics.

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## 1. Objectives

The main objective of this three year research effort is to investigate the large-signal characteristics of a heterojunction bipolar transistor (HBT) and to apply the knowledge gained to improve both the HBT device and circuit design.

Through innovative approaches for large-signal characterization and modelling, the following will be achieved:

- o Effective parameter extraction from DC and RF measurements to provide feedback to HBT device design.
- o Accurate large-signal measurement in the frequency domain, taking into account the effects of harmonic magnitudes and phases.
- o Non-linear equivalent circuit model for efficient de-embedding from DC and RF characteristics.

## 2. Progress

During the first year of this research effort, many types of measurements have been set up and performed to fully characterize the heterojunction bipolar transistor (HBT). The measurements include DC, RF, small signal, power and harmonic tests as will be described in the following. All measurements were performed on-wafer which eliminates substrate thinning, dicing and packaging and allows for rapid characterization. The devices characterized were GaAs/AlGaAs HBTs fabricated by the Air Force Wright Laboratory with either three  $1\mu \times 8\mu$  emitters, or a single  $1\mu \times 8\mu$  emitter. The Al concentration at the base emitter junction was graded from 0.3 to 0.0. The substrate thickness was  $625\mu\text{m}$ .

A simple yet accurate ten-element equivalent circuit model has been developed for the HBT. The model has seven fixed elements and three bias-dependent elements which vary in a nonlinear fashion. This bias dependant model is accurate to within 2% over the entire bias range. The power and harmonic characteristics of the heterojunction bipolar transistor have also been accurately modeled. Pulsed DC and thermal measurements have also been accomplished to determine the junction temperature and understand its effects on device characteristics.

### 2.1 DC and RF Characterization

The equipment used for DC characterization and device biasing includes an HP4142 Semiconductor Parametric Analyzer equipped with three source and monitoring units of either voltages or currents. For high frequency measurements the equipment used included an HP8510-B, a 40GHz network analyzer with a two port S-parameter test-set, and a HP70206A

26GHz spectrum analyzer. Calibration of the test equipment was performed on-wafer using a Tektronix calibration substrate.

The DC characterization performed on the HBTs included common emitter I-V, collector and base current vs base voltage, floating collector, and breakdown measurements. All of these result in parameters used as starting points for determining RF equivalent circuit parameters. They are also used to define operating points for high frequency measurements as shown in Figure 1 where the X's on the common emitter plot indicate the bias points for RF measurements.

Complete S-parameter measurements from 0.5 to 40GHz have been performed for three HBT devices from the same wafer under various bias conditions. Figure 2 shows a representative plot of S11 and S22 on a Smith chart. Figure 3 illustrates the magnitude of the forward current gain,  $|H_{21}|$ , and the power gain with their respective cutoff frequencies essentially equal, i.e.,  $f_T = f_{max} = 33\text{GHz}$  for this particular transistor. For the bias dependent model, complete sets of S-parameters were measured over the full range of operating conditions from the saturation region to cutoff as shown in Figure 1. Figure 4 shows a plot of  $|H_{21}|$  for several bias conditions.  $|H_{21}|$  can be seen to drop off at both high (bias point 6) and low currents (bias point 1). This nonlinear gain reduction is an important feature included in the bias dependent modeling.  $f_T$  is seen to change with bias, especially near cut-off. This behavior is expected from the dependence of depletion region capacitance on bias at both the base-emitter and base-collector junctions.

## 2.2 Bias-Dependent Equivalent Circuit Modeling

Based on the above measurements, a high frequency equivalent circuit model of the HBT was developed. As a beginning, a simple microwave equivalent circuit was proposed in which several elements are permitted to vary with bias. The goal was to identify elements that vary significantly with bias which are critical to the HBT large-signal behavior. As expected, these bias dependent elements are closely related to the intrinsic device characteristics instead of parasitics.

The CAD tools used for the modeling include HSPICE [1] a SPICE derivative capable of extracting bipolar junction transistor parameters from DC data. The LIBRA circuit simulator [2] is also used to perform the bulk of the modeling work. Libra is a powerful microwave equivalent circuit simulator and unlike SPICE, computations are performed in the frequency domain to yield fast and accurate steady state responses. A feature used extensively is the capability of LIBRA to fine tune (optimize) a circuit to better fit measured S-parameter data.

Figure 5 shows the proposed microwave equivalent circuit model for a particular device. A complete DC analysis was performed, and S-parameter measurements were taken at more than ten bias points in the forward-active region. The parasitic resistances  $R_b$  and  $R_e$  in the model were extracted from a plot of base and collector current vs base voltage. Approximate values

of  $R_c$  and  $R_{cb}$  were extracted from the common emitter saturation characteristics. From RF characteristics, a starting value of  $C_{cb}$  was obtained from the previously measured  $f_{max}$  and  $f_T$ :

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_{cb}}} \quad (1)$$

$R_o$  and  $C_{ce}$  were estimated from the output reflection coefficient  $S_{22}$ .  $C_{cb}$  was estimated from the base emitter junction area and the doping levels at the junction. A starting value of  $C_{cb}=1pF$  was used for the  $1\mu \times 8\mu$  device.

From these initial values the equivalent circuit was optimized to fit S-parameter data at the many bias conditions allowing all elements to be optimized. This was performed to three devices to determine which element values were most sensitive to changes in bias conditions.

Figure 6 shows the relative change of each element with bias. From this experiment it was apparent that the large-signal behavior is dominated by the change of  $C_{cb}$ ,  $R_{eb}$ , and  $\beta$ , therefore the final model was one in which all elements are held constant except for these three. The fixed elements were assigned the average value from the sensitivity analysis above. The final model with the fixed element values is shown in Figure 5.

Starting all from the same model elements, the circuit was optimized separately for each bias condition allowing only  $C_{cb}$ ,  $R_{eb}$ , and  $\beta$  to vary. The result is a set of data for these three elements versus the different bias conditions. Figure 7 is a combined graph of these three elements versus the collector current bias. The expected nonlinear behavior of  $C_{cb}$  and  $R_{eb}$  is apparent, and the typical  $\beta$  reduction at high and low current levels is seen. The increasing and decreasing behavior of  $C_{cb}$  and  $R_{eb}$  are consistent with bipolar transistor theory and are fit very well by the exponential expressions:

$$R_{eb} = K_r \exp\left(\frac{I_c}{-n_r}\right) \quad (2)$$

$$C_{cb} = K_c \exp\left(\frac{I_c}{+n_c}\right) \quad (3)$$

A representative plot of modeled and measured data is shown in Figure 8. Agreement is very good over the entire frequency range. The calculated mean squared error for all bias points is below two percent.

### 2.3 Pulsed DC Measurements

For on-wafer measurements even at moderate power levels, un-packaged and un-thinned HBTs exhibit significant thermal effects. For the HBT, the undesirable thermal effects result in a reduction of gain. To analyze the thermal effects and simulate packaged device performance, pulsed DC measurements have been performed to reduce the average power hence junction temperature.

Figure 9 shows the measurement configuration where a pulsed base voltage was adjusted to obtain a desired base current. The average HBT base current was measured through  $R_{Diff}$  and the average collector current was measured through  $V_c$ .  $C_c$  supplies the current pulse to the collector while keeping the voltage fixed.  $R_1$  and  $R_2$  are added to reduce reflections and  $R_e$  allows monitoring of the emitter current waveform through an oscilloscope.

For the particular HBTs measured, an average thermal time constant of  $5\mu s$  was found. At pulse widths of  $1\mu s$ , thermal effects were found to be negligible, so actual pulsed I-V data was taken at this pulse width. A duty cycle of 1/2 was used, which reduces the total power through the device by 1/2. Figure 10 shows the common emitter I-V characteristics of the single  $1\mu \times 8\mu$  emitter HBT on a  $625\mu$  substrate. For this configuration, the pulsed measurement significantly reduced the thermal effects.

### 2.4 Thermal Measurements

It is important to obtain the base-emitter junction temperature for a range of power levels to fully quantify the thermal effects of the HBT. The base emitter voltage ( $V_{be}$ ) was used as a temperature reference because at a constant base current,  $V_{be}$  is a function of temperature. The dependence of  $V_{be}$  on temperature was obtained empirically and used to find the junction temperature during normal operation. This temperature dependence was compared to theoretical calculations and found to be accurate.

To obtain the temperature dependence of  $V_{be}$ , several low power I-V measurements were performed on a device heated to a variety of known temperatures from  $27^\circ C$  to  $190^\circ C$ . These calibration measurements were performed on the device mounted in a metal TO-package which was connected to a Teflon test fixture and placed in an oven. Figure 11 shows the base current characteristics at the different ambient temperatures. This dependence was used to find the junction temperature of the device operated at different power levels in a room temperature ambient. A common emitter measurement was taken at  $I_b = 4mA$  and  $V_{be}$  was monitored as the device power increased with the rising  $V_{cc}$ . The junction temperature for each power level was calculated from  $V_{be}$ . The resulting thermal resistance is  $1700^\circ C/W$ .

This thermal resistance from the temperature measurements was compared with a three-dimensional heat flow analysis [3]. The exact solution of this heat flow was formulated in terms

of infinite sums, and evaluated up to three digit accuracy. Since the actual chip was not square as required in the simulation, a maximum and minimum dimension were chosen, and the resulting range of possible temperatures are shown in Figure 12 along with the measured junction temperature. The previous measured junction temperature values are seen to fall well within the range of this heat flow analysis.

From the determined junction temperature, the change in current gain,  $\beta$ , is shown in Figure 13 to be a approximately a linear function of temperature. The gain is reduced almost 10% at a junction temperature of 150°C.

## 2.5 Power and Harmonic Large Signal Modeling

On-wafer power and harmonic measurements have been performed on HBT's with three  $1\mu \times 8\mu$  emitter fingers. Since the measurements were performed before substrate thinning, a pulsed measurement technique was developed to reduce the heating effects. As a result, the maximum output power exceeded 2 W/mm which is twice the value under CW conditions.

The measurements were taken at 5.5 GHz and the RF input was modulated with a pulse width of  $5\mu\text{s}$  with 20% duty cycle. A common-emitter configuration was used with a constant base voltage bias. Both Class A and Class AB bias conditions were used. The class A results (shown in Figure 14) have higher gain, but lower output power than the class AB results. The power-added efficiency is lower than 20% for both classes. These low efficiencies are due to the fixed  $50\Omega$  loading condition, and higher efficiencies are expected under optimum matching conditions.

Harmonic measurements have also been performed for a range of input power levels. To model the harmonic behavior of the HBT as well as general S-parameter response, a technique is being developed for building a large-signal model based entirely on S-parameter measurements. Empirical formulas are proposed to characterize the nonlinear conductances, current gain, and transit time allowing them to be extracted from small-signal S-parameter measurements. The model has five nonlinear elements: both base-emitter and base-collector resistances and capacitances, and the transconductance. The nonlinear elements are extracted by fitting bias-dependent small-signal element values to the empirical expression for its corresponding nonlinear large-signal element.

For a  $50\Omega$  loading condition the class A harmonic measurements and simulations are shown in Figure 15. The simulation produced excellent agreement to the measurement. From a time domain analysis of the large-signal model, the saturation of output power is seen to occur when the collector voltage swings from the cutoff to the saturation region; this is where the second and fourth harmonics are reduced to a local minimum.

## 2.6 Conclusion

Extensive DC and RF characterization has been performed for evaluation of device performance



and extraction of model elements. Pulsed DC and high temperature measurements have also been performed to analyze the thermal resistance and relate actual junction temperature to device performance.

A simple yet accurate ten-element equivalent circuit model has been developed for the HBT. The model has seven fixed elements and three bias-dependent elements which vary in a nonlinear fashion. All three elements have simple functional forms making them efficient for simulations; two are simple exponentials while the third is an inverted "U". The model is compared to measured S-parameter data with less than 2% mean square error.

A large-signal model is being developed by using empirical forms for five nonlinear elements. This model has been compared to power and harmonic measurements yielding excellent agreement. This model has also been used to verify time domain explanations for power saturation and harmonic variations with increasing input power.

## 2.7 Future Work

Work will continue relating the bias-dependence of model elements to the large-signal microwave response. Actual large-signal microwave measurements will be taken, and currently a pulsed technique is being developed. The model will be compared and modified based on the measured results.

Further DC pulsed measurements will be performed with duty cycles less than 10% and pulse widths less than  $1\mu\text{s}$  to ensure that the pulsed power is not raising the junction temperature significantly. Additional thermal measurements are also required to include higher temperature measurements, and to reduce power during these measurements. A pulsed technique will be used where the junction is first self-heated at normal operating conditions, then the junction temperature is measured by a short lower power pulse. From these measurements, a knowledge of the junction temperature at any DC bias condition can be obtained, as well as the junction temperature within the large-signal RF voltage swing. With accurate knowledge of the junction temperature during operating conditions, modeling of the thermal effects of the HBT can be achieved. This model will be incorporated into the overall large-signal model. To test its versatility, model results will be compared to devices of varying size and physical structure. Devices with thinned substrates will also be tested to verify thermal model predictions.

## 2.8 References

- <sup>1</sup> Meta-Software, Inc: HSPICE-H9001D, 1990 by Meta-Software, Inc., USA.
- <sup>2</sup> EEsof: Libra<sup>™</sup> version 2.0, 1989 by EEsof, Inc., USA.
- <sup>3</sup> Lindsted, R.D., and Surty, R.J., "Steady-State Junction Temperatures of Semiconductor Chips," *IEEE Trans. Electron Devices*, vol. 19, no. 1 (1972), p. 41.

### 3. Publications

Macpherson, A.K.; Behboudi, D.; Hwang, J.C.M.; and Micek, G. 1990. Modeling the epitaxial growth process of gallium arsenide. Proceedings of the ninth IEEE international electronics manufacturing technology symposium, Washington, DC, October 1-3, 1990.

Mah, M.Y.; King, J.M.; Worley, R.D.; Gillespie, J.; Neidhard, R.A.; W.L. Melvin; and Hwang, J.C.M. 1990. Quantitative analysis of mask misalignment and its effect on device performance. Technical digest of IEEE gallium arsenide integrated circuit symposium, New Orleans, Louisiana, October 7-10, 1990, pp. 313-315.

W.L. Melvin; and Hwang, J.C.M. 1991. Automated pattern recognition of wafer test data. In Digest of papers U.S. conference on GaAs manufacturing technology, April 7-10, Reno, Nevada, 1991, pp. 109-112.

Hwang, J.C.M.; 1991. MBE technology and MIMIC (Invited). MIMIC Tri-service Epitaxial Workshop. Arlington, VA, April 23-24, 1991.

Hwang, J.C.M.; and Macpherson, A.K. 1991. Modeling and simulation of compound semiconductor heterostructures. DARPA Digital GaAs Technology Review. Reston, VA, April 23-24, 1991.

Whitefield, D.S.; 1991. Large Signal Characterization and Modeling of Heterojunction Bipolar Transistors. Master's Thesis, Lehigh University. May 1991.

#### **Manuscripts in preparation planned for later submission:**

Wei, C.J.; Whitefield, D.S.; Hwang, J.C.M. Large Signal Modeling of Heterojunction Bipolar Transistors. Microwave Theory and Techniques.

Wei, C.J.; Whitefield, D.S.; Hwang, J.C.M. Direct Extraction of GaAs-AlGaAs HBT Intrinsic and Parasitic Element Values. Microwave Theory and Techniques.

#### **Presentations:**

Whitefield, D.S. Equivalent Circuit Modeling of a Heterojunction Bipolar Transistor. Wright Laboratory, Wright Patterson AFB, Ohio. July 1990.

Whitefield, D.S. Thermal effect in Heterojunction Bipolar Transistors. Lehigh University, Bethlehem PA. August 1990.

Whitefield, D.S. Large Signal Characterization and Modeling of Heterojunction Bipolar Transistors. Lehigh University, Bethlehem PA. May 1991.

#### **4. Professional Personnel**

**Dr. J.C.M. Hwang**

Professor of Electrical Engineering and

Director of Compound Semiconductor Technology Laboratory, Lehigh University.

**Dr. C.J. Wei**

Research Scientist, Compound Semiconductor Technology Laboratory, Lehigh University.

**D.S. Whitefield**

Graduate Student and Research Assistant.

M.S., Electrical Engineering, Lehigh University, 1991. Thesis: Large Signal Characterization and Modeling of Heterojunction Bipolar Transistors.

#### **5. Interactions**

Dr. Hwang is a consultant to the Air Force Wright Laboratory in the areas of MIMIC processing and material/device correlation. Dr. Hwang spends 20% of his time at Wright Laboratory and both written and oral progress reports on HBTs are provided regularly to Dr. Chern Huang and his colleagues. The HBT devices used for this work were fabricated at Wright Laboratory using their in-house MBE process.

D.S. Whitefield is a Second Lieutenant in the Air Force currently on a four year educational delay to complete his Ph.D. degree in Electrical Engineering. In July 1990, D.S. Whitefield spent one week at the Air Force Wright Laboratory discussing microwave device fabrication, characterization, and modeling.

#### **6. Inventions**

There have been no inventions for this report period (DD Form 882 Attached).

# REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on Reverse Side.)

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## SECTION I - SUBJECT INVENTIONS

"SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

b. NAME(S) OF INVENTOR(S) (Last, first, MI)	TITLE OF INVENTION(S)	5. DISCLOSURE NO., PATENT APPLICATION SERIAL NO. OR PATENT NO.	4. ELECTION TO FILE PATENT APPLICATIONS				6. CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER	
			(1) United States		(2) Foreign			
			(a) Yes	(b) No	(a) Yes	(b) No	(1) Yes	(2) No
None								

EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

9. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED	
(1) Title of Invention	(2) Foreign Countries of Patent Application
(1) (a) Name of Inventor (Last, first, MI)	
(b) Name of Employer	
(c) Address of Employer (Include ZIP Code)	

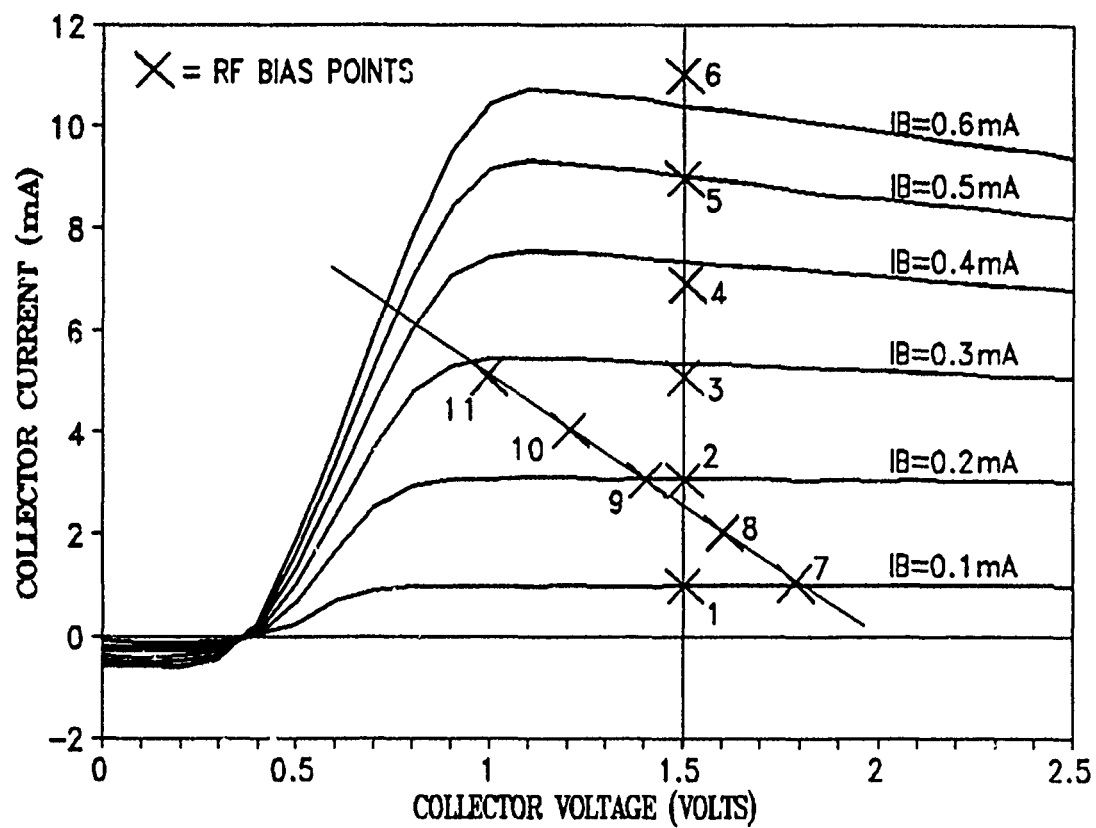
## SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

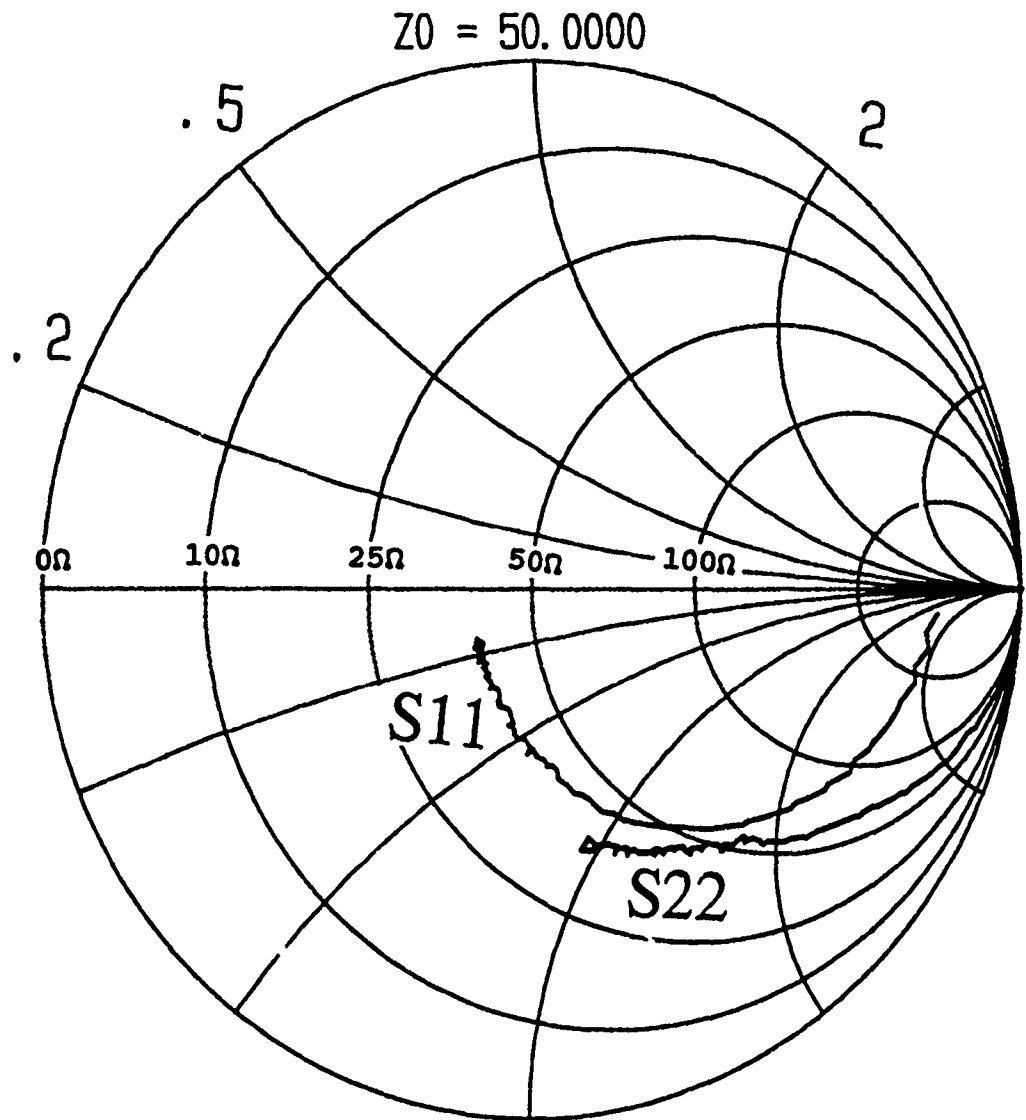
b. NAME OF SUBCONTRACTOR(S)	c. ADDRESS (Include ZIP Code)	c. SUBCONTRACT NO.(S)	d. DFAR "PATENT RIGHTS"		e. DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S)	f. SUBCONTRACT DATES (YYMMDD)	
			(1) Clause Number	(2) Date (YYMM)		(1) Award	(2) Estimated Completion
None							

## SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if Small Business or Non Profit organization) (X appropriate box)	
a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, first, MI) John M. Cheezum Jr.	c. I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.
b. TITLE Director, Office of Research and Sponsored Programs	d. SIGNATURE <i>Thomas J. Yeardley for DMC</i> e. DATE SIGNED 7/2/91

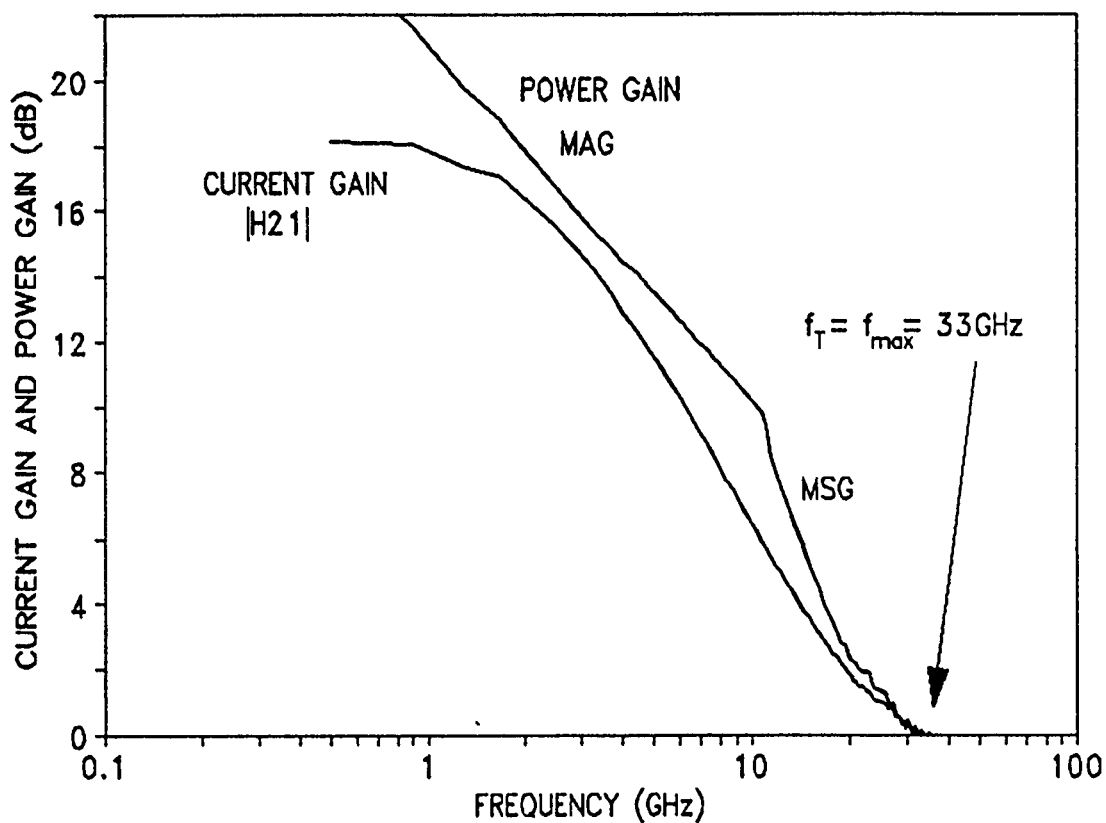


**Figure 1.** Common emitter response of an HBT.  
Bias points for RF measurements are also indicated.

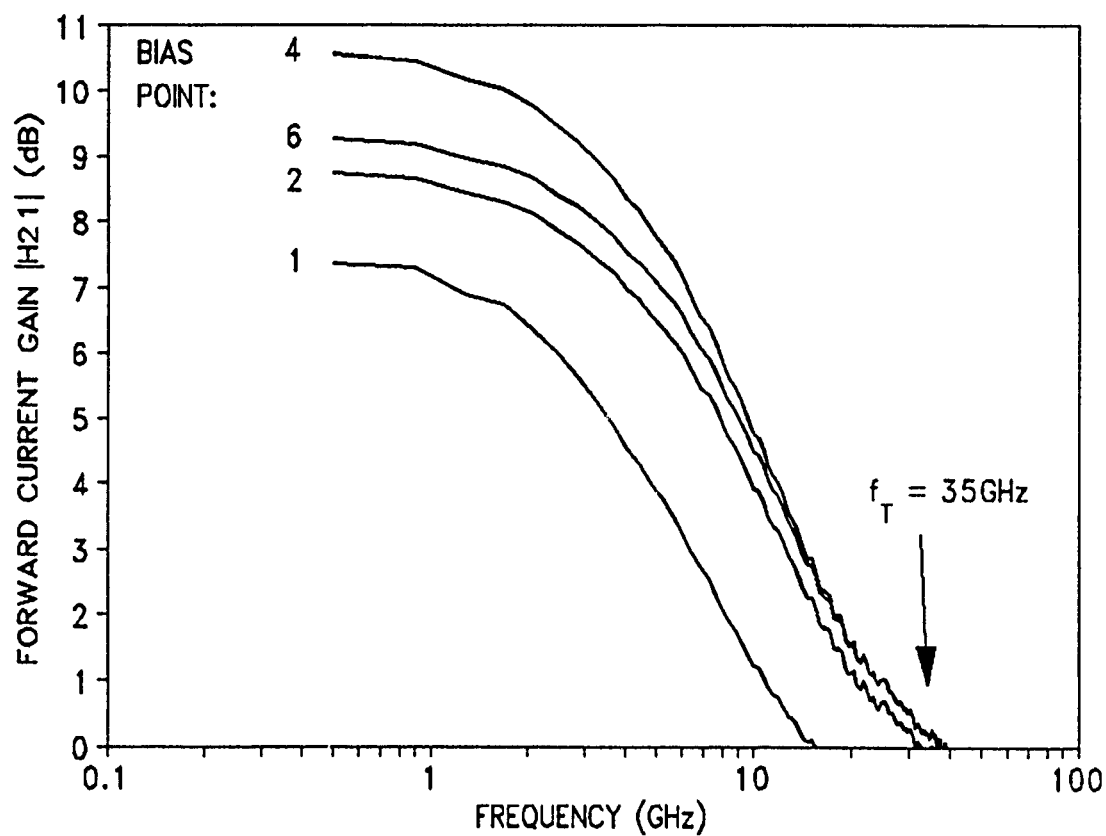


**Figure 2.** HBT reflection coefficients.

Input reflection ( $S_{11}$ ) and output reflection ( $S_{22}$ ) give the input and output complex impedances at microwave frequencies.  $S_{11}$  and  $S_{22}$  are swept from 0.5GHz to 40GHz (right to left).

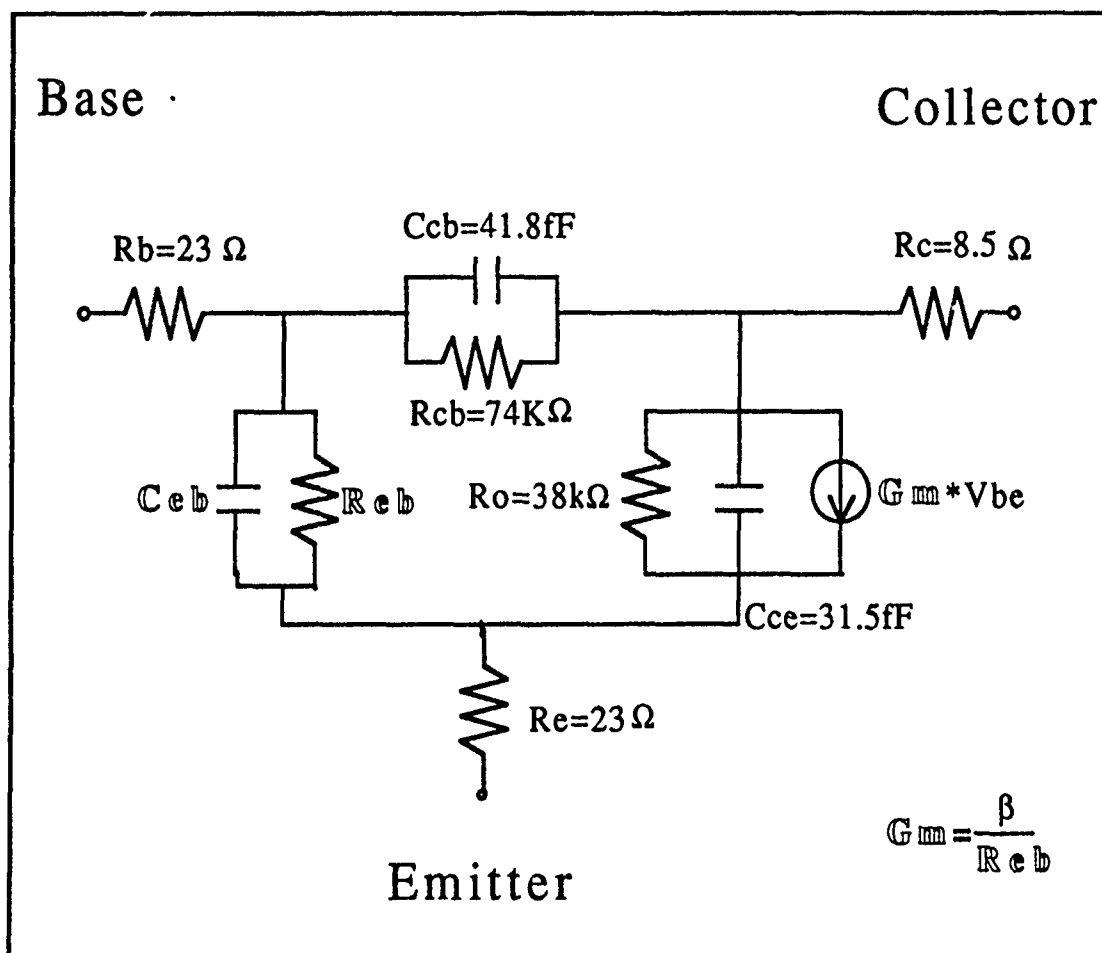


**Figure 3.** Forward current gain and power gain. Forward current gain ( $|H_{21}|$ ) has a unity gain at  $f_T = 33\text{GHz}$ . Power Gain (MSG and MAG) has a cutoff at  $f_{max} = 33\text{GHz}$  also.



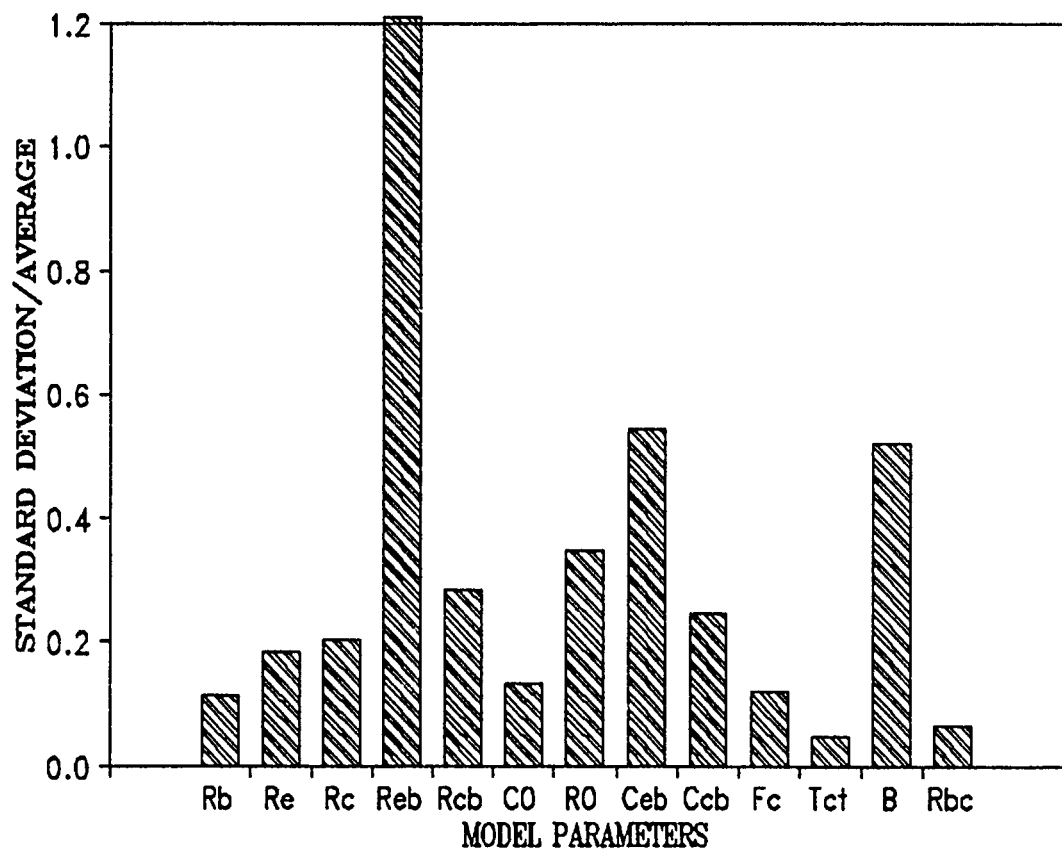
**Figure 4.** RF current gain for various bias points.  
Current gain drops at low and high currents as in DC measurements.





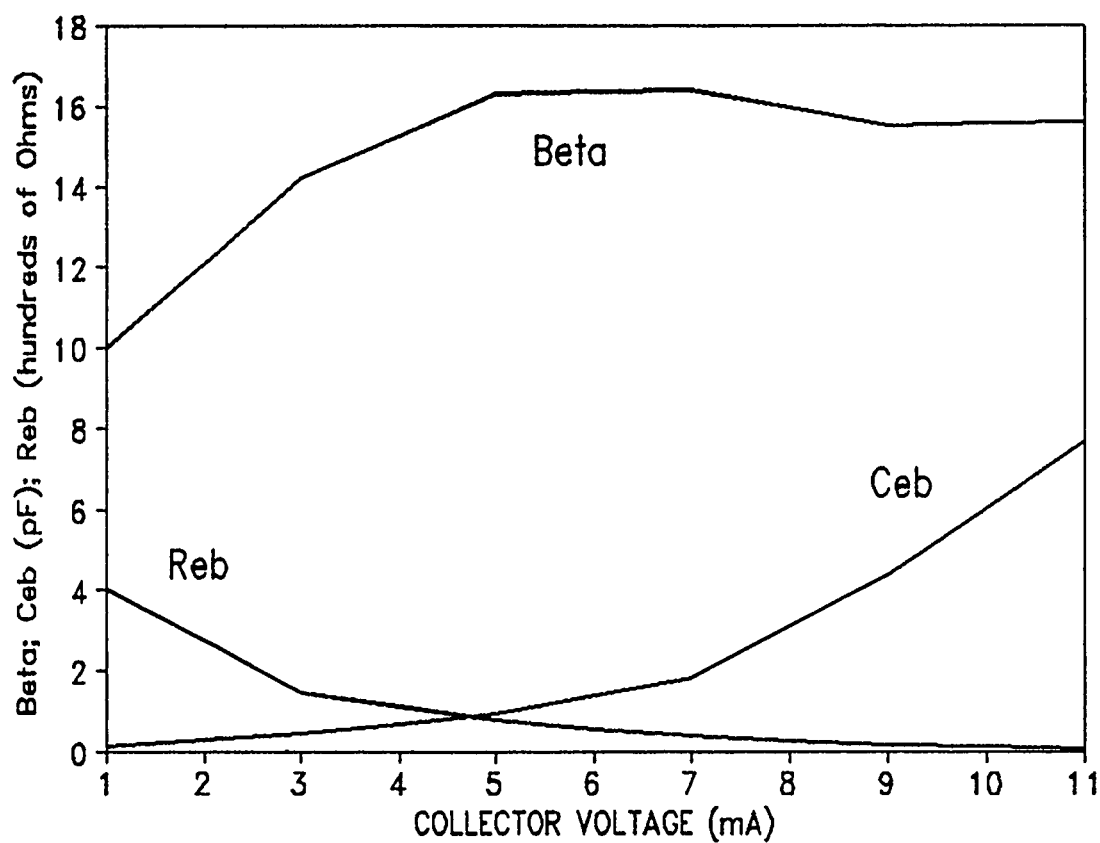
**Figure 5.** Final bias dependent model with element values.

$R_{eb}$ ,  $C_{eb}$  and  $\beta$  are allowed to vary with bias while the remainder of the elements are fixed as noted.



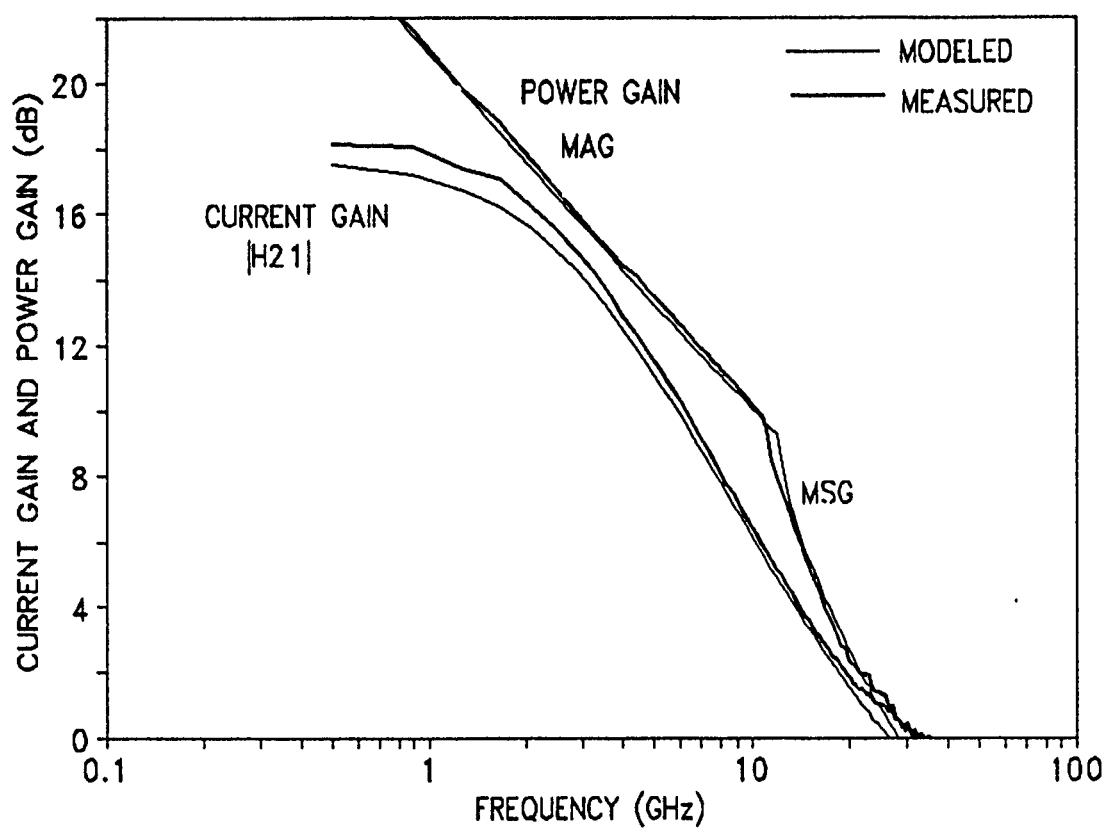
**Figure 6.** Variation of model parameters with bias.

Ceb, Reb, and  $\beta$  are seen to vary the greatest with bias. All others will be held constant in the final analysis.

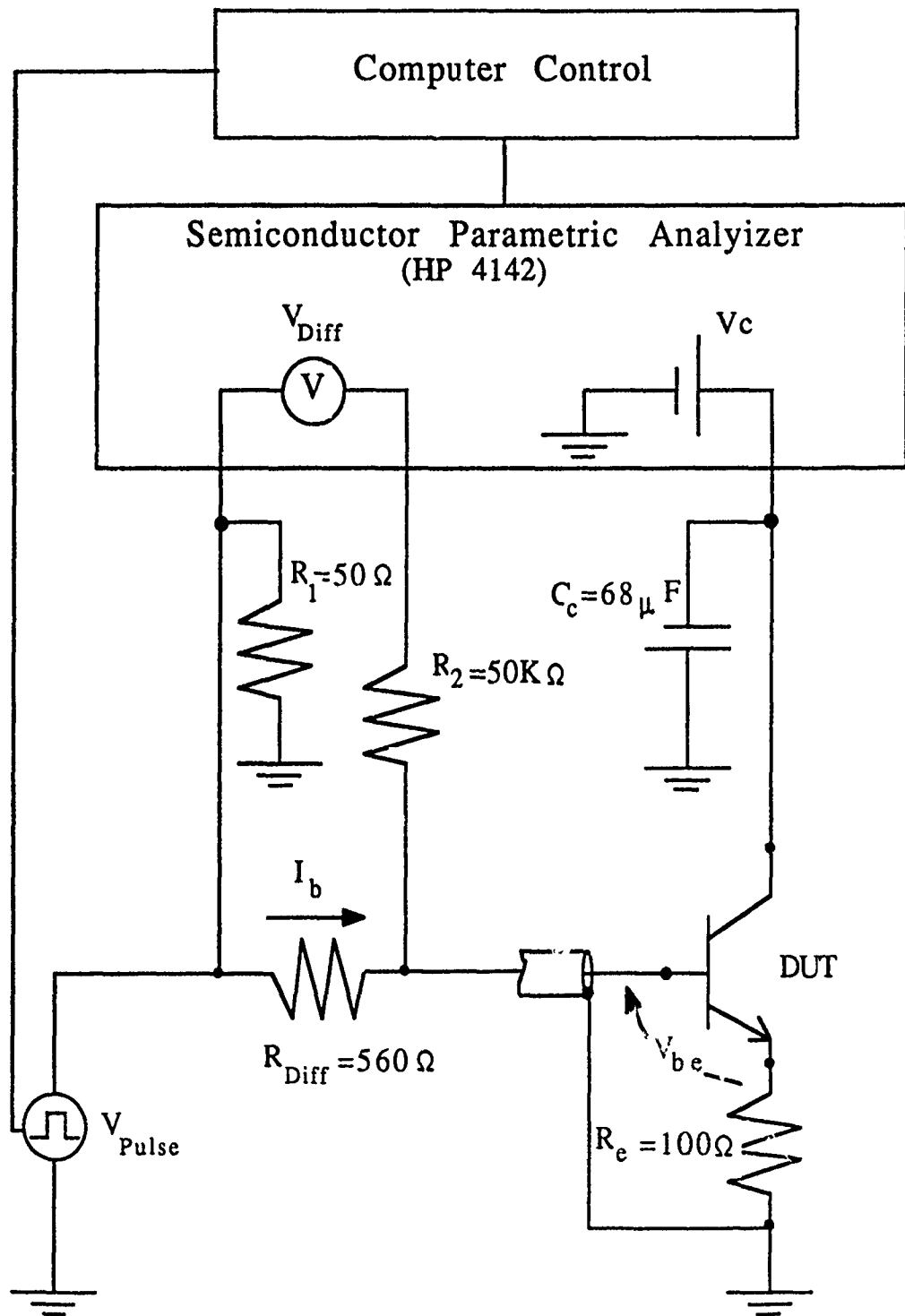


**Figure 7.** Bias dependence of key nonlinear elements.

All three elements which are allowed to vary with bias show non-linear dependence on the collector current. Reb and Ceb are essentially exponential functions, while  $\beta$  shows the typical reduction at high and low currents.

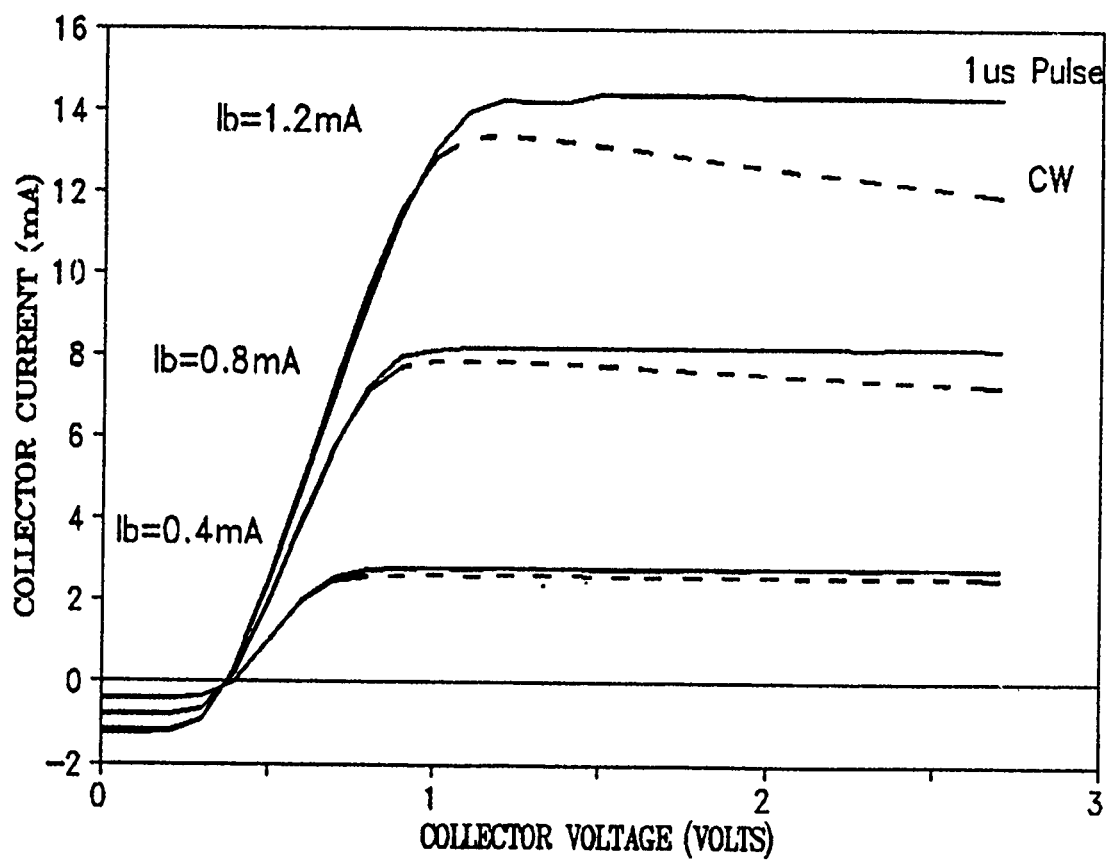


**Figure 8.** Modeled versus measured current and power gains. Forward current gain ( $|H_{21}|$ ) and power gain (MAG and MSG) show excellent agreement to measured data.

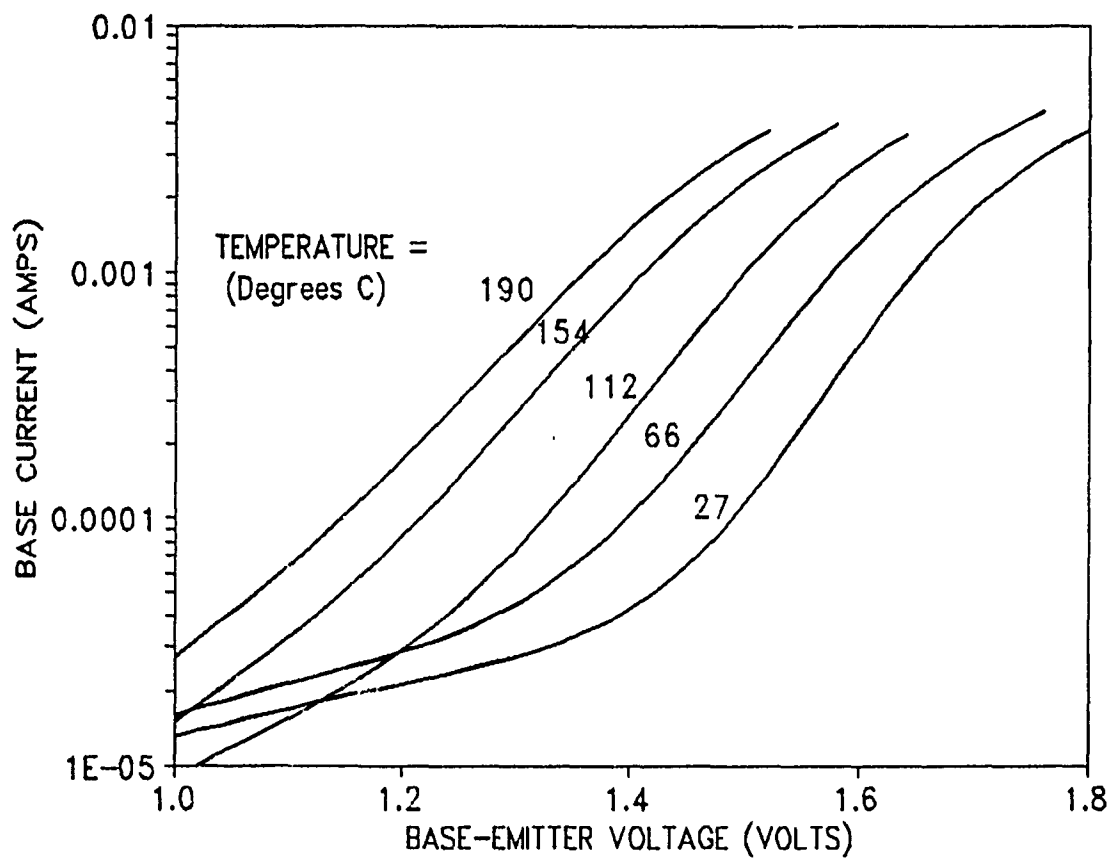


**Figure 9.** Pulsed measurement setup.

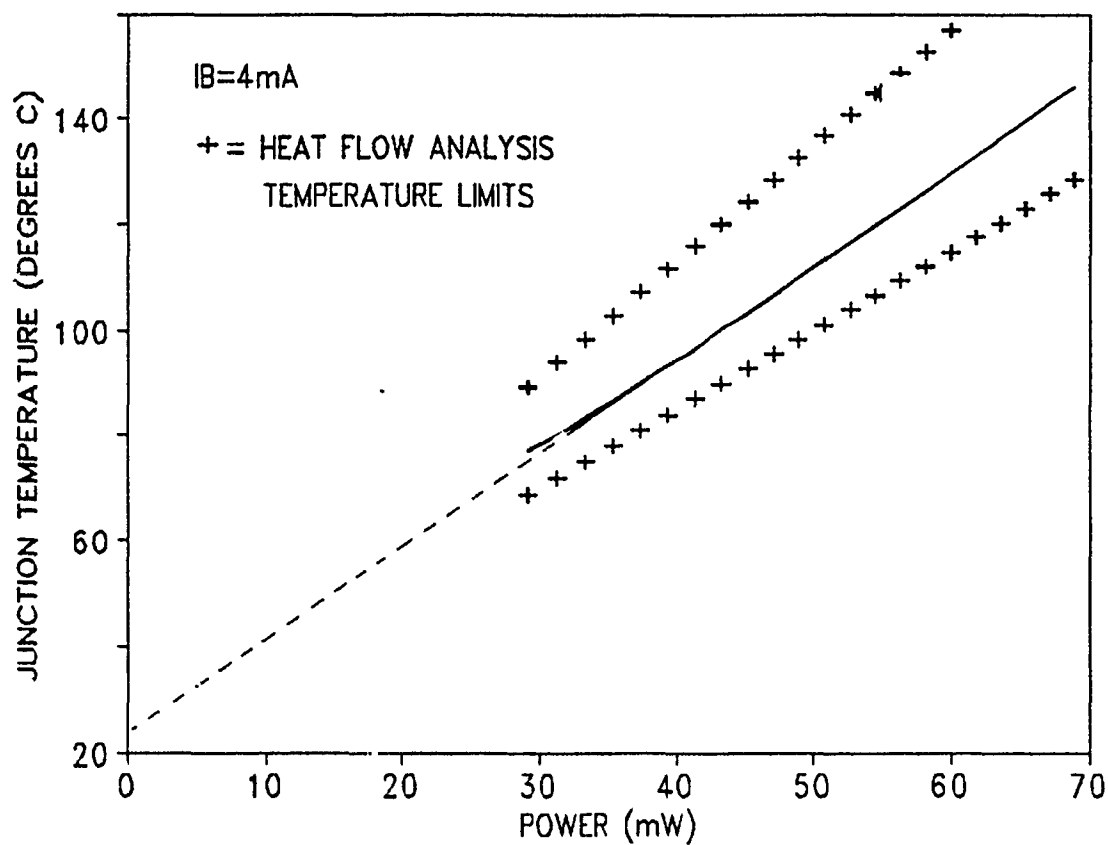
Pulses of constant current are applied to the base of the HBT and the average collector current is measured. The actual pulsed collector current value is calculated from the known duty cycle.



**Figure 10.** Pulsed I-V characteristics.  
Thermal effects are significantly reduced with a  $1\mu\text{s}$  pulsed base current.

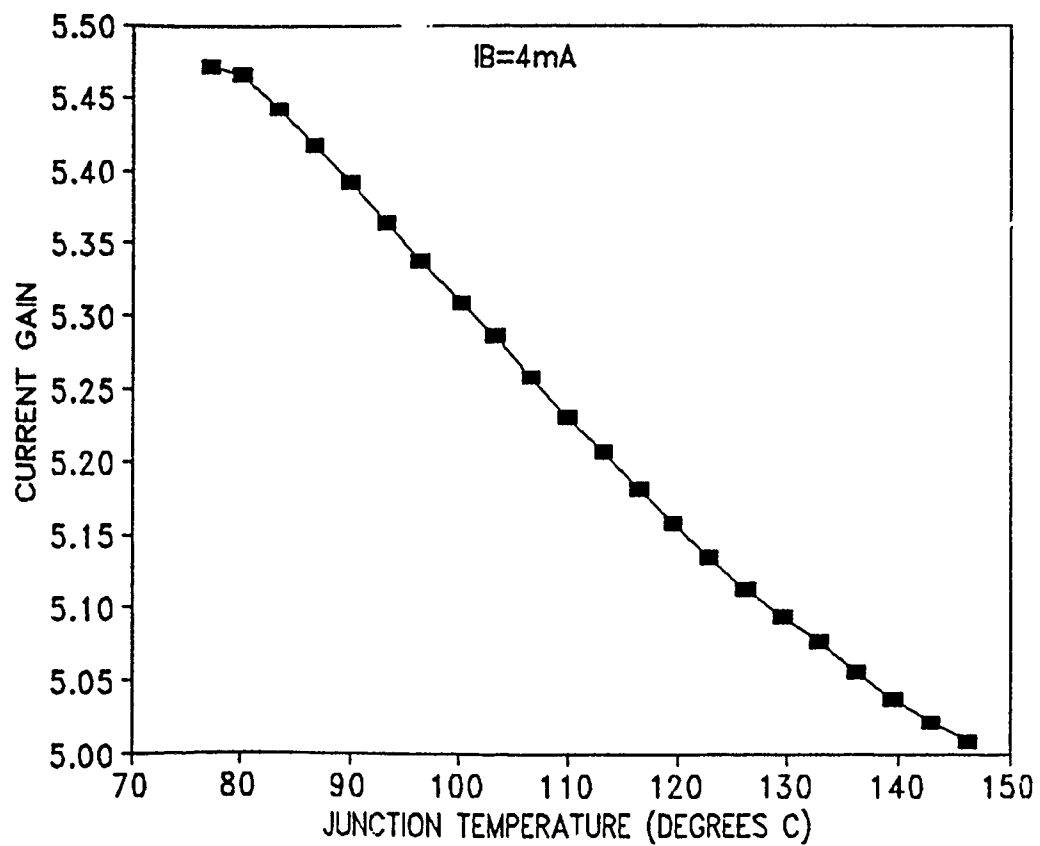


**Figure 11.** Dependence of base current on  $V_{be}$  and ambient temperature. The base current has a strong and predictable dependence on temperature.

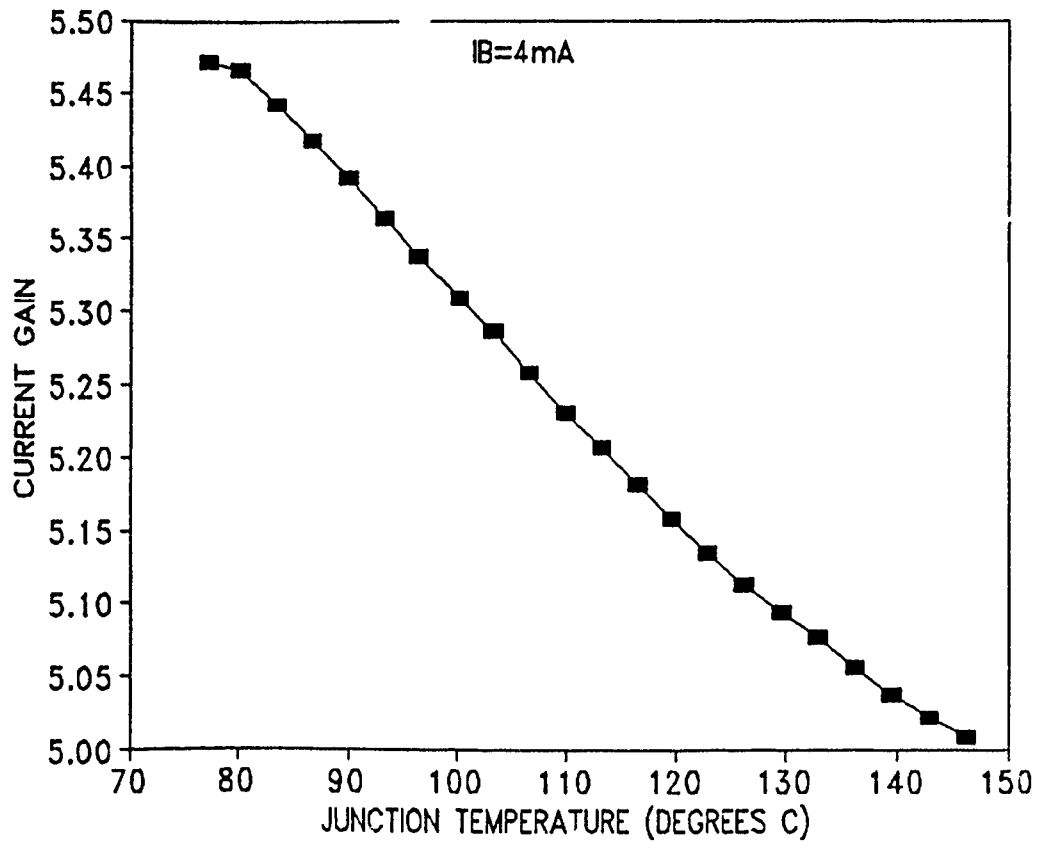


**Figure 12.** Junction temperature comparison to chip model.  
The calibrated junction temperature falls within the maximum and minimum temperatures as computed from the chip dimensions.

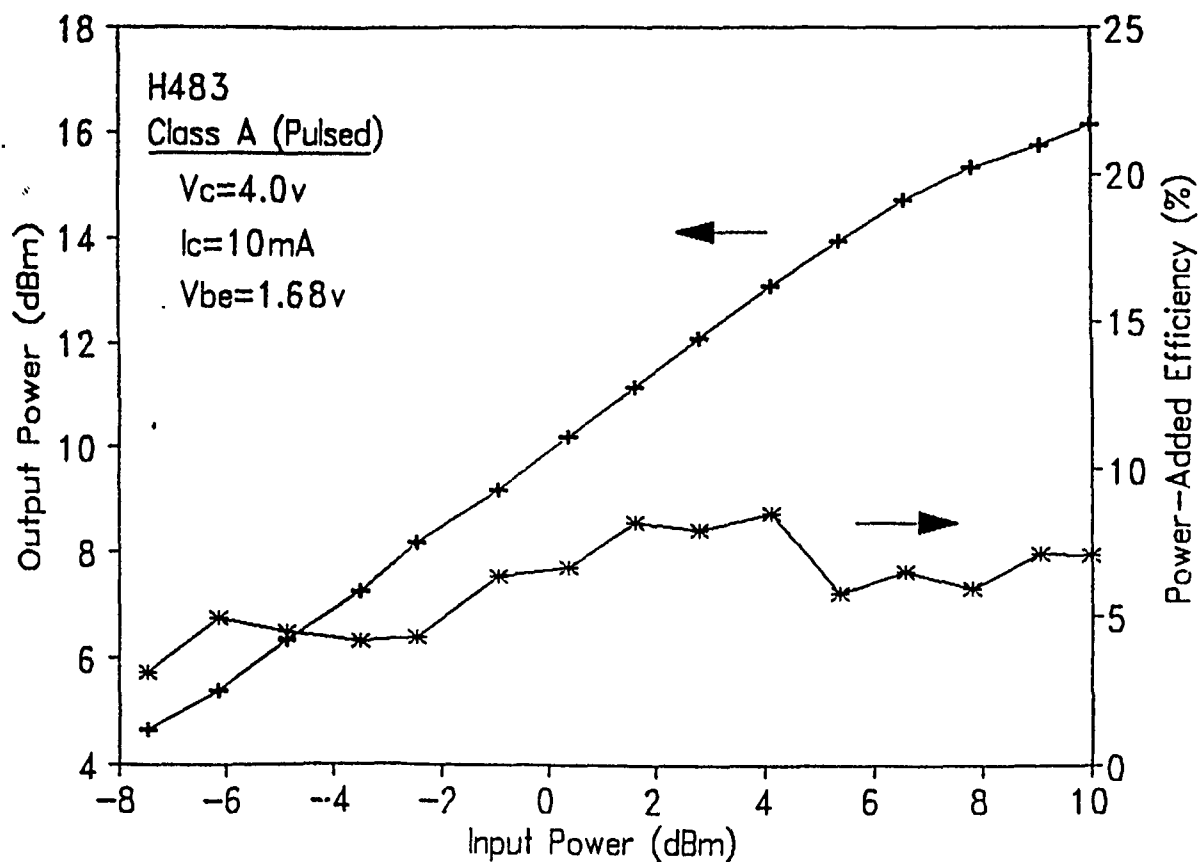




**Figure 13.** Current gain versus temperature.  
The current gain reduction is almost linear with temperature.

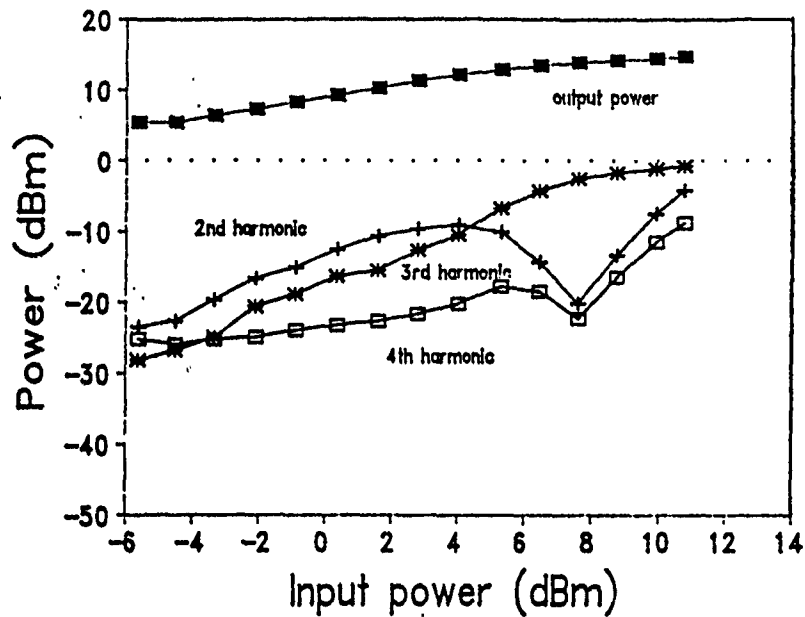


**Figure 13.** Current gain versus temperature.  
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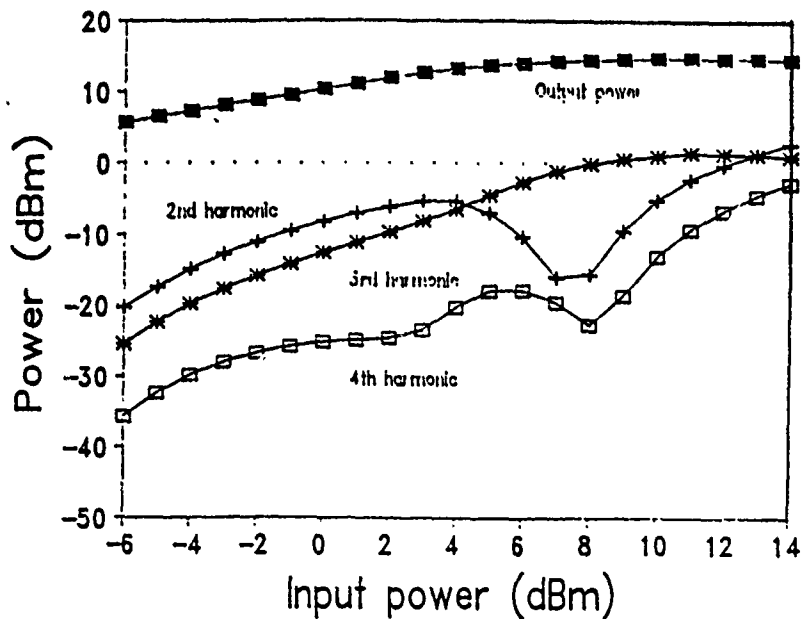


**Figure 14.** HBT output power and efficiency.  
Measurement is obtained for class A operation with  $50\Omega$  loading condition. Optimum impedance matching would increase efficiency.

Measured data: No.428  $V_c=3V$ ,  $I_{co}=10mA$



Simulated results:  $V_c=3V$   $I_{co}=10mA$



**Figure 15.** Harmonic measurement and simulation. Measurement and simulation are for class a operation and  $50\Omega$  loading condition. Output power saturation is due to signal swings into cutoff and saturation regions, this also corresponds to the 2nd and 4th harmonic minimums.